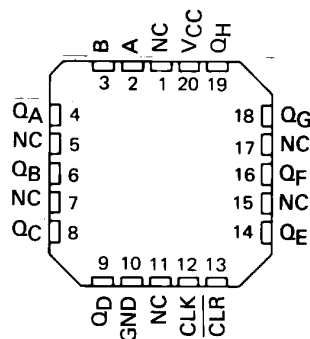


## MARCH 1974 — REVISED MARCH 1988

- SN54164, SN54LS164 . . . J OR W PACKAGE  
SN74164 . . . N PACKAGE  
SN74LS164 . . . D OR N PACKAGE  
(TOP VIEW)

Pinout diagram for the 74VHC00 hex inverters. The package is shown with pins 1 through 14. Pin 1 is labeled A, pin 2 is B, pin 3 is QA, pin 4 is QB, pin 5 is QC, pin 6 is QD, and pin 7 is GND. Pin 14 is VCC, pin 13 is QH, pin 12 is QG, pin 11 is QF, pin 10 is QE, pin 9 is CLR, and pin 8 is CLK.

**SN54LS164 . . . FK PACKAGE**  
**(TOP VIEW)**



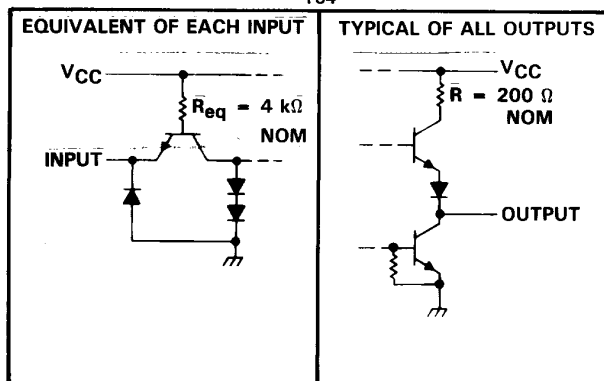
These 8-bit shift registers feature gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup-time requirements will be entered. Clocking occurs on the low-to-high-level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

The SN54164 and SN54LS164 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74164 and SN74LS164 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

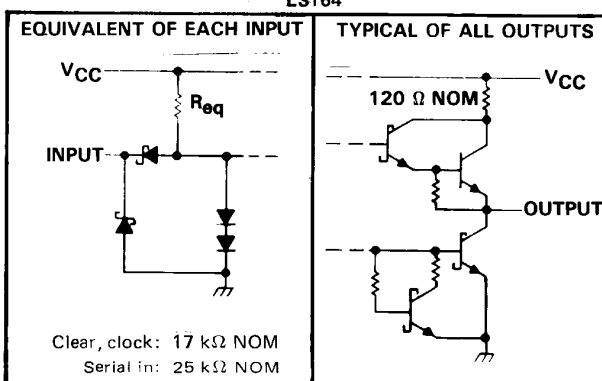
INPUTS			OUTPUTS		
CLEAR	CLOCK	A B	Q <sub>A</sub>	Q <sub>B</sub>	... Q <sub>H</sub>
L	X	X X	L	L	L
H	L	X X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>H0</sub>
H	↑	H H	H	Q <sub>An</sub>	Q <sub>Gn</sub>
H	↑	L X	L	Q <sub>An</sub>	Q <sub>Gn</sub>
H	↑	X L	L	Q <sub>An</sub>	Q <sub>Gn</sub>

$Q_{An}, Q_{Gn}$  = the level of  $Q_A$  or  $Q_G$  before the most-recent  $\uparrow$  transition of the clock; indicates a one-bit shift.

## '164

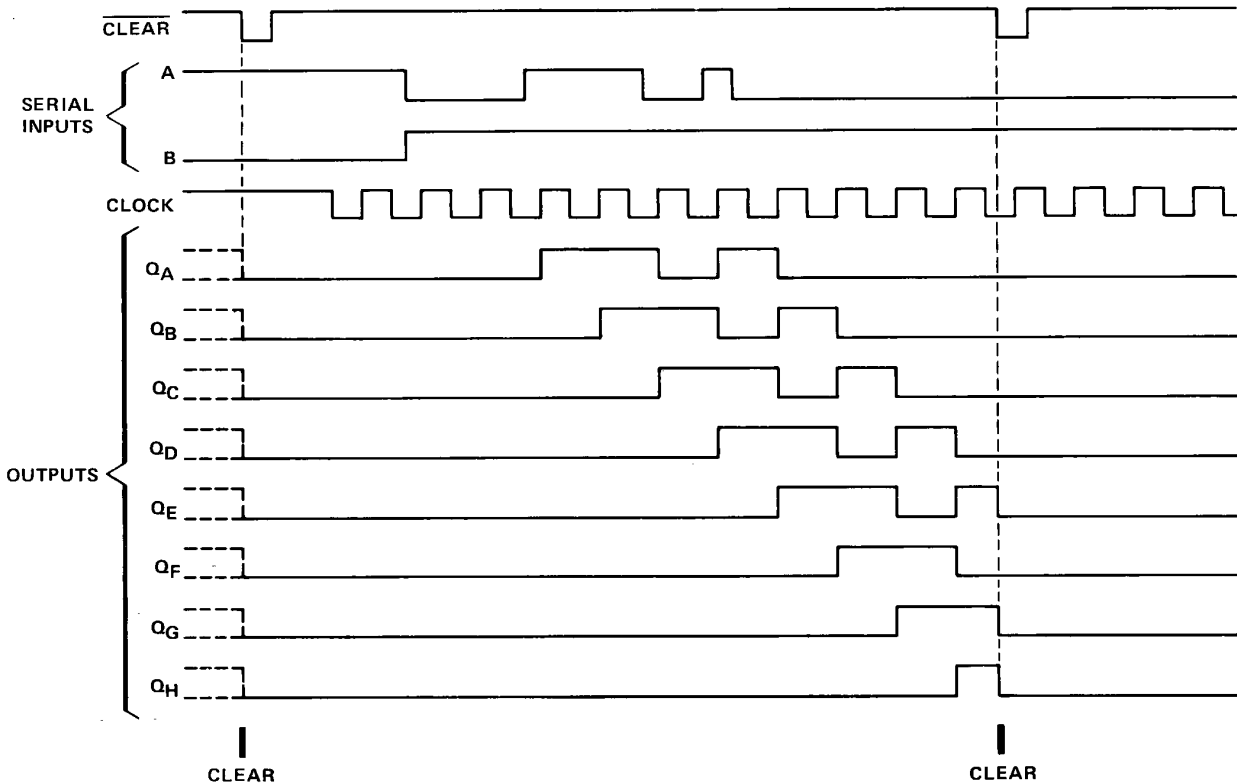


'LS164

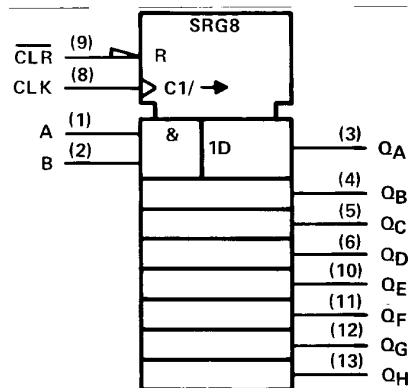


# **SN54164, SN54LS164, SN74164, SN74LS164** **8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS**

typical clear, shift, and clear sequences



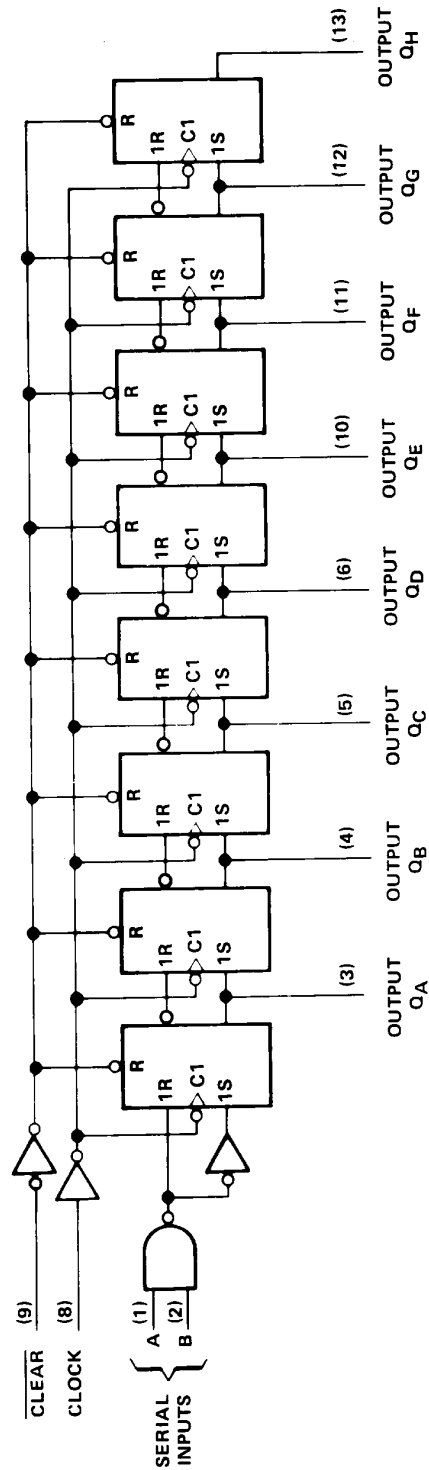
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, N, and W packages.

**SN54164, SN54LS164, SN74164, SN74LS164**  
**8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS**

logic diagram (positive logic)



2

TTL Devices

# SN54164, SN74164

## 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54164	–55°C to 125°C
SN74164	0°C to 70°C
Storage temperature range	–65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54164			SN74164			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$			–400			–400	$\mu$ A
Low-level output current, $I_{OL}$			8			8	mA
Clock frequency, $f_{clock}$	0		25	0		25	MHz
Width of clock or clear input pulse, $t_W$	20			20			ns
Data setup time, $t_{SU}$ (see Figure 1)	15			15			ns
Data setup time, $t_{SU}$ (Clear Inactive) (see Figure 1)	20			20			ns
Data hold time, $t_H$ (see Figure 1)	5			5			ns
Operating free-air temperature, $T_A$	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54164			SN74164			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{IH}$ High-level input voltage		2			2			V
$V_{IL}$ Low-level input voltage				0.8			0.8	V
$V_{IK}$ Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			–1.5			–1.5	V
$V_{OH}$ High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = 0.8 \text{ V}, I_{OH} = -400 \mu\text{A}$	2.4	3.2		2.4	3.2		V
$V_{OL}$ Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = 0.8 \text{ V}, I_{OL} = 8 \text{ mA}$		0.2	0.4		0.2	0.4	V
$I_I$ Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V},$			1			1	mA
$I_{IH}$ High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40			40	$\mu$ A
$I_{IL}$ Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			–1.6			–1.6	mA
$I_{OS}$ Short-circuit output current§	$V_{CC} = \text{MAX}$	–10		–27.5	–9		–27.5	mA
$I_{CC}$ Supply current	$V_{CC} = \text{MAX}, V_I(\text{clock}) = 0.4 \text{ V}$		30			30		mA
	See Note 2 $V_I(\text{clock}) = 2.4 \text{ V}$		37	54		37	54	

† For conditions shown at MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

§ Not more than two outputs should be shorted at a time.

NOTE 2:  $I_{CC}$  is measured with outputs open, serial inputs grounded, and a momentary ground, then 4.5 V, applied to clear.

switching characteristics,  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{max}$ Maximum clock frequency	$C_L = 15 \text{ pF}$	25	36		MHz
$t_{PHL}$ Propagation delay time, high-to-low-level Q outputs from clear input	$C_L = 15 \text{ pF}$		24	36	ns
	$C_L = 50 \text{ pF}$		28	42	
$t_{PLH}$ Propagation delay time, low-to-high-level Q outputs from clock input	$C_L = 15 \text{ pF}$	8	17	27	ns
	$C_L = 50 \text{ pF}$	10	20	30	
$t_{PHL}$ Propagation delay time, high-to-low-level Q outputs from the clock input	$C_L = 15 \text{ pF}$	10	21	32	ns
	$C_L = 50 \text{ pF}$	10	25	37	

# SN54LS164, SN74LS164

## 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS164	–55°C to 125°C
SN74LS164	0°C to 70°C
Storage temperature range	–65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

### recommended operating conditions

		SN54LS164			SN74LS164			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.7			0.8	V
$I_{OH}$	High-level output current			–0.4			–0.4	mA
$I_{OL}$	Low-level output current			4			8	mA
$f_{clock}$	Clock frequency	0		25	0		25	MHz
$t_w$	Width of clock or clear input pulse	20			20			ns
$t_{su}$	Data setup time (See Figure 1)	15			15			ns
$t_{su}$	Clear inactive setup time (See Figure 1)	20			20			ns
$t_h$	Data hold time (See Figure 1)	5			5			ns
$T_A$	Operating free-air temperature	–55		125	0		70	°C

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		SN54LS164		SN74LS164		UNIT
			MIN	TYP‡	MAX	MIN	
V <sub>IK</sub>	V <sub>CC</sub> = MIN, I <sub>I</sub> = –18 mA		–1.5		–1.5		V
V <sub>OH</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = MAX, I <sub>OH</sub> = –0.4 mA		2.5	3.5	2.7	3.5	V
V <sub>OL</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = MAX	I <sub>OL</sub> = 4 mA	0.25	0.4	0.25	0.4	V
		I <sub>OL</sub> = 8 mA			0.35	0.5	
I <sub>I</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V		0.1		0.1		mA
I <sub>IH</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V		20		20		μA
I <sub>IL</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V		–0.4		–0.4		mA
I <sub>OS</sub>	V <sub>CC</sub> = MAX		–20	–100	–20	–100	mA
I <sub>CC</sub>	V <sub>CC</sub> = MAX, See Note 3		16	27	16	27	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 3:  $I_{CC}$  is measured with outputs open, serial inputs grounded, the clock input at 2.4 V, and a momentary ground, then 4.5 V applied to clear.

### switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{max}$ Maximum clock frequency		25	36		MHz
$t_{PHL}$ Propagation delay time, high-to-low-level Q outputs from clear input	$R_L = 2 \text{ k}\Omega, C_L = 15 \text{ pF},$		24	36	ns
$t_{PLH}$ Propagation delay time, low-to-high-level Q outputs from clock input	See Figure 1		17	27	ns
$t_{PHL}$ Propagation delay time, high-to-low-level Q outputs from clock input			21	32	ns

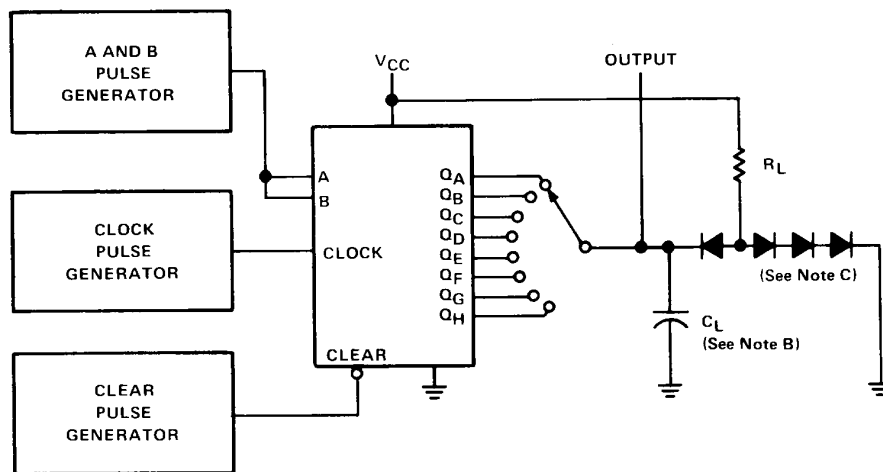
2

TTL Devices

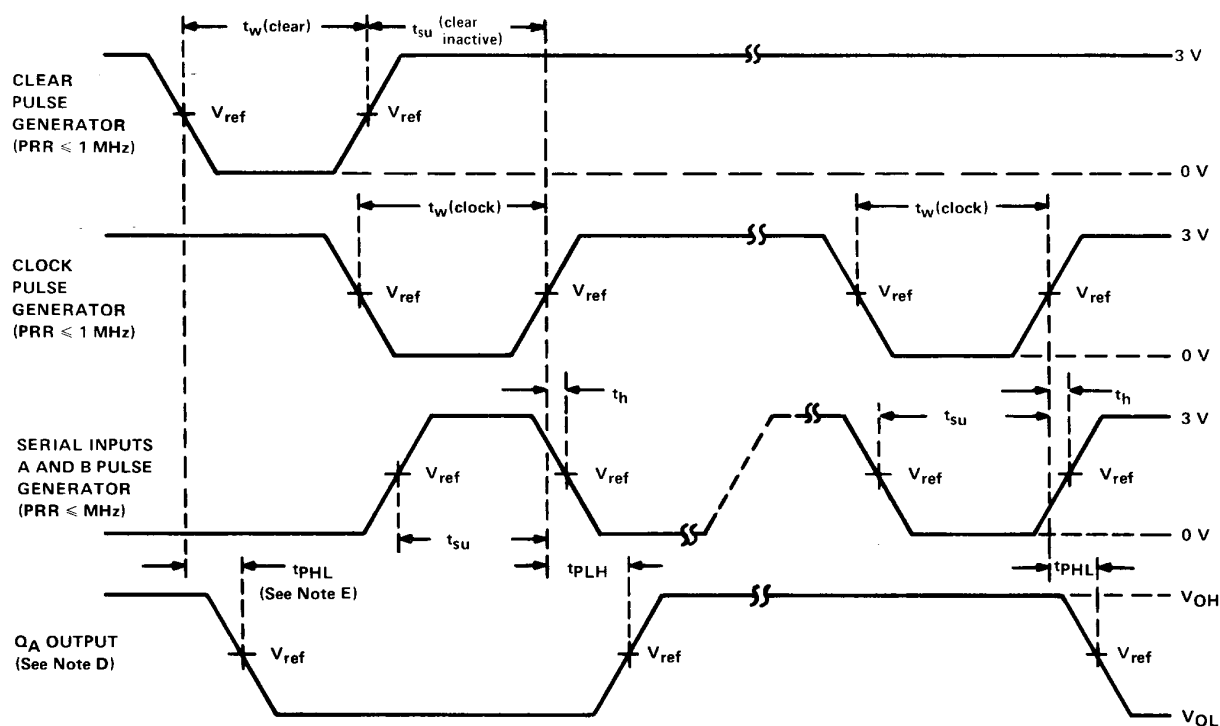
# SN54164, SN54LS164, SN74164, SN74LS164

## 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

### PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

- NOTES: A. The pulse generators have the following characteristics: duty cycle  $\leq 50\%$ ,  $Z_{out} \approx 50 \Omega$ ; for '164,  $t_r \leq 10$  ns,  $t_f \leq 10$  ns; and for 'LS164,  $t_r \leq 15$  ns,  $t_f \leq 6$  ns.
- B.  $C_L$  includes probe and jig capacitance.
- C. All diodes are 1N3064 or equivalent.
- D.  $Q_A$  output is illustrated. Relationship of serial input A and B data to other Q outputs is illustrated in the typical shift sequence.
- E. Outputs are set to the high level prior to the measurement of  $t_{PHL}$  from the clear input.
- F. For '164,  $V_{ref} = 1.5$  V; for 'LS164,  $V_{ref} = 1.3$  V.

FIGURE 1—SWITCHING TIMES

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
JM38510/30605B2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30605B2A	<a href="#">Samples</a>
JM38510/30605BCA	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30605BCA	<a href="#">Samples</a>
JM38510/30605BCA	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30605BCA	<a href="#">Samples</a>
JM38510/30605BDA	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30605BDA	<a href="#">Samples</a>
JM38510/30605BDA	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30605BDA	<a href="#">Samples</a>
JM38510/30605SCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30605SCA	<a href="#">Samples</a>
JM38510/30605SCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30605SCA	<a href="#">Samples</a>
JM38510/30605SDA	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30605SDA	<a href="#">Samples</a>
JM38510/30605SDA	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30605SDA	<a href="#">Samples</a>
M38510/30605B2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30605B2A	<a href="#">Samples</a>
M38510/30605B2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30605B2A	<a href="#">Samples</a>
M38510/30605BCA	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30605BCA	<a href="#">Samples</a>
M38510/30605BCA	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30605BCA	<a href="#">Samples</a>
M38510/30605BDA	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30605BDA	<a href="#">Samples</a>
M38510/30605BDA	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30605BDA	<a href="#">Samples</a>
M38510/30605SCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30605SCA	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
M38510/30605SCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30605SCA	<a href="#">Samples</a>
M38510/30605SDA	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30605SDA	<a href="#">Samples</a>
M38510/30605SDA	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30605SDA	<a href="#">Samples</a>
SN54LS164J	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54LS164J	<a href="#">Samples</a>
SN54LS164J	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54LS164J	<a href="#">Samples</a>
SN74LS164D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS164	<a href="#">Samples</a>
SN74LS164D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS164	<a href="#">Samples</a>
SN74LS164DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS164	<a href="#">Samples</a>
SN74LS164DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS164	<a href="#">Samples</a>
SN74LS164DRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS164	<a href="#">Samples</a>
SN74LS164DRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS164	<a href="#">Samples</a>
SN74LS164N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS164N	<a href="#">Samples</a>
SN74LS164N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS164N	<a href="#">Samples</a>
SN74LS164NE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS164N	<a href="#">Samples</a>
SN74LS164NE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS164N	<a href="#">Samples</a>
SN74LS164NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS164	<a href="#">Samples</a>
SN74LS164NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS164	<a href="#">Samples</a>
SN74LS164NSRE4	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS164	<a href="#">Samples</a>
SN74LS164NSRE4	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS164	<a href="#">Samples</a>
SNJ54LS164FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS 164FK	<a href="#">Samples</a>



Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54LS164FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS 164FK	<a href="#">Samples</a>
SNJ54LS164J	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS164J	<a href="#">Samples</a>
SNJ54LS164J	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS164J	<a href="#">Samples</a>
SNJ54LS164W	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS164W	<a href="#">Samples</a>
SNJ54LS164W	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS164W	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54LS164, SN54LS164-SP, SN74LS164 :**

- Catalog : [SN74LS164](#), [SN54LS164](#)
- Military : [SN54LS164](#)
- Space : [SN54LS164-SP](#)

**NOTE:** Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS164DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LS164NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS164DR	SOIC	D	14	2500	853.0	449.0	35.0
SN74LS164NSR	SO	NS	14	2000	853.0	449.0	35.0

## TUBE



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
JM38510/30605B2A	FK	LCCC	20	1	506.98	12.06	2030	NA
M38510/30605B2A	FK	LCCC	20	1	506.98	12.06	2030	NA
SN74LS164D	D	SOIC	14	50	506.6	8	3940	4.32
SN74LS164N	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS164N	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS164NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS164NE4	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54LS164FK	FK	LCCC	20	1	506.98	12.06	2030	NA

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK





**J 14**

## GENERIC PACKAGE VIEW

**CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

**J0014A****PACKAGE OUTLINE****CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

**NOTES:**

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.



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# EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only  
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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